PATENT ABSTRACTS OF JAPAN

(11) Publication number: 62093954 A

(43) Date of publication of application: 30.04.87

(51) Int. CI

H01L 21/76 H01L 21/306 H01L 29/72

(21) Application number: 60233340

(22) Date of filing: 21.10.85

(71) Applicant:

OKI ELECTRIC IND CO LTD

(72) Inventor:

ISHIKIRIYAMA MAMORU

(54) MANUFACTURE OF DIELECTRIC ISOLATION SUBSTRATE

(57) Abstract:

PURPOSE: To reduce warpage a substrate may come to be provided with during its manufacture by a method wherein single-crystal islands in a single-crystal semiconductor substrate are divided from each other by dielectric regions.

CONSTITUTION: A plurality of grooves 15 is formed on the surface of a single- crystal semiconductor substrate 11 with a masking layer 13 serving as a mask. The masking layer 13 works again in a process wherein an isolating/insulating film 16 is formed on the inner walls of the groove 15. The masking layer 13 is then removed for the exposure of the substrate surface between the grooves 15. A semiconductor layer 17 is formed on said exposed substrate surface and in the groove 15. The entirety of the semiconductor layer 17 is subjected to annealing for conversion into a single-crystal layer with a single-crystal section in a substrate surface region 17b on the semiconductor layer 17 serving as the nucleus. A semiconductor layer 18 is epitaxially grown, which continues until the groove 15 on the single crystal semiconductor layer 17 is filled. Removal is performed starting from the surface side, for the removal of the semiconductor layers 17 and 18, which continues until the substrate surface is exposed. The semiconductor layers 17 and 18 are allowed to remain only in the groove 15.

COPYRIGHT: (C)1987,JPO&Japio

